Technical Program at a Glance

Day-1: 19th December, 2012 (Wednesday) Venue: BESU, Kolkata			
9:00 AM – 9:30 AM	Registration		
9:30 AM – 10:00 AM	Inauguration		
10:00 AM – 11:40 AM	**Keynote Speech – 1** Cross-Layer Error Awareness for Embedded Systems Speaker: Nikil Dutt, Chancellor's Professor of CS and EECS, Center for Embedded Computer Systems, University of California, Irvine, USA		
	Keynote Speech – 2 Synthesis of Reversible Circuits using Decision Diagrams Speaker: Rolf Drechsler, DFKI Bremen and University of Bremen, Germany		
11:40 AM – 12:00 AM	TEA BREAK		
12:00 AM – 1:20 PM	**Session A1** Emerging Technology and System Design (ETS-1)	**Session B1** Analog/Mixed Signal System Design (AMS-1)	**Session C1** Digital System Design and Validation (DSD-1)
1:20 PM – 2:20 PM	LUNCH BREAK		
2:20 PM – 3:00 PM	**Keynote Speech – 3** Edge of Insanity: Modeling & Validating Complex Systems Speaker: Arjun Kapur, Director, Software Development Intel Mobile and Communications Group, USA		
3:00 PM – 3:30 PM	TEA BREAK		
3:30 PM – 5:00 PM	Special Session on Reversible Circuit Synthesis (RCS)		
5:00 PM – 6:00 PM	Poster Presentation Session		

Day 2: 20th December, 2012 (Thursday) Venue: BESU, Kolkata			
8:00 AM – 9:00 AM	Registration		
9:00 AM – 10:00 AM	**Keynote Speech – 4** Demystifying Board-Level Test and Diagnosis Speaker: Krishnendu Chakrabarty, Duke University, USA		
10:00 AM – 11:20 AM	**Session A2** Embedded System Design (ESD-1)	**Session B2** Software System and Applications Design (SSD)	**Session C2** Digital System Design and Validation (DSD-2)
11:20 AM – 11:50 AM	TEA BREAK		
11:50 AM – 1:10 PM	**Session A3** Emerging Technology and System Design (ETS-2)	**Session B3** Power Aware System Design (PSD)	**Session C3** Digital System Design and Validation (DSD-3)
1:10 PM – 2:00 PM	LUNCH BREAK		
2:00 PM – 3:00 PM	**Keynote Speech – 5** Digital Signal Processing: Road to the Future Speaker: Sanjit K. Mitra, Research Professor of Electrical & Computer Engg, University of California, Santa Barbara, USA		
3:00 PM – 3:30 PM	TEA BREAK		
3:30 PM – 5:20 PM	**Session A4** Emerging Technology and System Design (ETS-3)	**Session B4** Analog/Mixed Signal System Design (AMS-2)	**Session C4** Digital System Design and Validation (DSD-4)
5:20 PM – 6:00 PM	Networking / Break		
6:00 PM – 9:00 PM	Cultural Programme + Banquet Dinner		

Day 3: 21st December, 2012 (Friday) Venue: BESU, Kolkata			
8:00 AM – 9:00 AM	Registration		
9:00 AM – 10:00 AM	**Keynote Speech – 6** Linear Circuits: A Measurement Based Approach Speaker: Shankar Bhattacharyya, Robert M. Kennedy Professor of Electrical Engineering, Texas A&M University, USA		
10:00 AM – 11:20 AM	**Session A5** Emerging Technology and System Design (ETS-4)	**Session B5** Wireless/Wired Communication Systems (WCS)	**Session C5** Digital System Design and Validation (DSD-5)
11:20 AM – 11:50 AM	TEA BREAK		
11:50 AM – 1:10 PM	**Session A6** Emerging Technology and System Design (ETS-5)	**Session B6** Embedded System Design (ESD-2)	**Session C6** Digital System Design and Validation (DSD-6)
1:10 PM – 2:00 PM	LUNCH BREAK		
2:00 PM – 3:00 PM	**Keynote Speech – 7** Top-down Synthesis Methodology for Flow-Based Microfluidic Biochips Speaker: Tsung-Yi Ho, Department of Computer Science and Information Engineering, National Cheng Kung University, Taiwan		
3:00 PM – 3:30 PM	TEA BREAK		
3:30 PM – 4:50 PM	**Session A7** Emerging Technology and System Design (ETS-6)	**Session B7** Digital System Design and Validation (DSD-7)	
5:00 PM – 5:30 PM	VALEDICTORY		

DAY 4: 22nd December, 2012 (Saturday) *Workshop on Nano-electronics and Biochips* Venue: Indian Statistical Institute, Calcutta	
9:00 AM – 10:00 AM	Registration
10:00 AM – 11:20 AM	**Lecture – 1** Efficient Neural Computing using Cellular Array of Magneto-Metallic Neurons Speaker: Kaushik Roy, Department of Electrical and Computer Engineering Purdue University, USA
11:20 AM – 11:50 AM	TEA BREAK
11:50 AM – 1:10 PM	**Lecture – 2** Dr. Kaushik Saha, ST Microelectronics
1:10 PM – 2:00 PM	LUNCH BREAK
2:00 PM – 3:20 PM	**Lecture – 3** Nanotechnology: Enabling the Future of Computing Speaker: Kota Murali, Chief Scientist and Program Director of Nanotechnology, IBM, India
3:20 PM – 3:50 PM	TEA BREAK
3:50 PM – 5:10 PM	**Lecture – 4** Design Automation for Digital Microfluidic Biochips: from Fluidic-Level toward Chip-Level Speaker: : Tsung-Yi Ho, Department of Computer Science and Information Engineering, National Cheng Kung University, Taiwan

Special Session on Reversible Logic Synthesis (RLS)

Michael K. Thomsen, Holger B. Axelsen and Robert Glück, "Cleaning Up: Garbage-Free Reversible Circuits by Design Languages

Gerhard W. Dueck, "Synthesis of Toffoli Networks: Status and Challenges"

D. Michael Miller and Zahra Sasanian, "Recent Developments on Mapping Reversible Circuits to Quantum Gate Libraries"

Session –B1

Analog/Mixed-Signal System Design (AMS-1)

101:Selvakumar Jayakumar, Vidhyacharan Bhaskar and Narandran S. FPGA Implementation of Efficient Parallel FIR Digital Filter Based on Fast FIR Algorithm

102:Rajasekar Rajendran and Ramakrishna P.V.. A Design of 6-bit125-MS/s SAR ADC in 0.13-µm Mixed mode RF CMOS Process

120:Sagar Mukherjee, Dipankar Saha, Posiba Mostafa, Sayan Chatterjee and Chandan Kumar Sarkar. A 4-bit Asynchronous Binary Search ADC for Low Power, High Speed Applications

Session-B4

Analog/Mixed-Signal System Design (AMS-2)

Embedded Tutorial: Strain Engineered MOSFETs for Low Power Digital Circuit Applications

Speaker: Prof. Sanatan Chattopadhaya, Calcutta University, Kolkata

27:Vasantha M. H. and Tonse Laxminidhi. 0.5 V, Low Power, 1 MHz Low Pass Filter in 0.18 µm CMOS Process

92:Laxmikandan Thangavelu and Ramakrishna P V. Design Space Exploration and Synthesis of CMOS Low Noise Amplifiers

Session-C1

Digital System Design and Validation (DSD-1)

24:Niras C V and Vinu Thomas. Systolic Variable Length Architecture of Discrete Fourier Transform for Long Term Evolution

79: Rohit Srivastava, Nandini Mudgil, Gaurav Gupta and Hemanta Mondal. SoC Time to market improvement through Device Driver Reuse: an industrial experience

127:Tapas Maiti, Subhadip Kundu, Arpita Dutta and Santanu Chattopadhyay. Confidence Based Power Aware Testing

Session-C2

Digital System Design and Validation (DSD-2)

85: Santanu Kumar Dash, Gayadhar Panda and Nirjharini Sahoo. Analysis and Operation of FPGA-Based Hybrid Active Power Filter for Harmonic Elimination in a Distribution System

94: Sumeet Agrawal, Pinalkumar Engineer, Rajbabu Velmurugan and Sachin Patkar. FPGA Implementation of Particle Filter based Object Tracking in Video

118: Swaminathan Kathirvel, Lakshminarayanan G and Ko Seok-Bum. High Speed Generic Network Interface for Network on Chip using Ping Pong Buffers

Session-C3

Digital System Design and Validation (DSD-3)

116:K. C. Cinnati Loi and Seok-Bum Ko. Improvements for High Performance Elliptic Curve Cryptosystem Processor over GF(2^163)

115:Fateme Naderpour and Seokbum Ko. Improved Design of High-Radix Signed-Digit Adders

146:Xingxing Jin and Seok-Bum Ko. GPU-based Parallel Implementation of SAR Imaging

Session-C4

Digital System Design and Validation (DSD-4)

32:Santhosh Keshavarapu, Saumya Jain and Manisha Pattanaik. A New Assist Technique to Enhance the Read and Write Margins of Low Voltage SRAM cell

75:Syed Ahmed, Sreehari V, Srinivas M.B, Sibi Abhram and Moorthy Muthukrishnan. A Modified Twin Precision Multiplier with 2D bypassing technique
114:Atin Mukherjee and Anindya Sundar Dhar. Design of a Self-reconfigurable Adder for Fault-tolerant VLSI Architecture

Session-C5

Digital System Design and Validation (DSD-5)

Embedded Tutorial: VLSI Design Verification: Technological Trends and Research Opportunities
Speaker: Ansuman Banerjee, Indian Statistical Institute, Kolkata

17: R.Uma Ramadass. Systolic FIR Filter Design with Various Parallel Prefix Adders in FPGA: Performance Analysis
97: Sandip Ghosh, Prokash Ghosh and Sourav Roy. Dynamic Sharing of On-Chip Scratchpad Memory on Embedded Platforms

Session-C6

Digital System Design and Validation (DSD-6)

Embedded Tutorial: Formal Verification in Informal Worlds
Speaker: Pallab Dasgupta, IIT Kharagpur, India

10: Deepak Chauhan, Manoj Sharma and Sharad Kumar. Post Silicon Validation of Digital Radio Interfaces
93: Kunal Banerjee, Chandan Karfa, Dipankar Sarkar and Chittaranjan Mandal. A Value Propagation Based Equivalence Checking Method for Verification of Code Motion Techniques

Session-C7

Digital System Design and Validation (DSD-7)

121: Subhramita Basak, Dipankar Saha, Sagar Mukherjee, Sayan Chatterjee and Chandan Kumar Sarkar. Design and Analysis of a Robust, High Speed, Energy Efficient 18 Transistor 1-bit Full Adder Cell, modified with the concept of MVT Scheme
60: S Sivanantham, Sarathkumar K, Jincy P Manuel, P S Mallick and J Raja Paul Pernibam. CSP-Filling: A New X-Filling Technique to Reduce Capture and Shift Power in Test Applications
130: Surajit Kumar Roy, Sobitri Chatterjee and Chandan Giri. Identifiing Faulty TSVs in 3D Stacked IC During Pre-bond Testing

Session-A2

Embedded System Design (ESD-1)

Embedded Tutorial: Embedded System Design for Assistive Systems
Speaker: Anupam Basu, Professor, Computer Science & Engineering Dept., IIT Kharagpur,

91: Hoang M. Le, Daniel Grosse and Rolf Drechsler. From Requirements and Scenarios to ESL Design in SystemC
123:Anirban De, Santwana Kumari, V.K. Khare, S.S. Pal, Anindya Sadhukhan, V.K. Meshram, S.K. Thakur and Subimal Saha. Design, Development and Testing of a DSP based Dynamic Voltage Restorer

Session-B6

Embedded System Design (ESD-2)

105:I. Hiteshwar Rao, Nafisa Ali Amir, Haresh Dagale and Joy Kuri. e-SURAKSHAK: A Cyber-Physical Healthcare System with Service Oriented Architecture

129:Vishal Shrivastav, Satya Gautam Vadlamudi, Partha Pratim Chakrabarti, Dipankar Das and Purnendu Sinha. Finding critical components in embedded control systems sensitive to quality-faults
131:Pradip Kumar Sahu, Ashish Sharma and Santanu Chattopadhyay. Application Mapping onto Mesh-of-Tree based Network-on-Chip using Discrete Particle Swarm Optimization

Session-A1

Emerging Technology and System Design (ETS-1)

81: Papiya Manna, Dipak Kumar Kole, Hafizur Rahaman, Debesh K. Das and Bhargab B. Bhattacharya. Reversible Logic Circuits Synthesis using Genetic Algorithm and Particle Swarm Optimization
117: Deepak Bharti and Abhijit Asati. Design of a Static Current Simulator Using Device Matrix Approach
148: Brijesh Kumar, B.K. Kaushik, and Y.S. Negi "Analysis of Contact Resistance Effect on Performance of Organic Thin FilmTransistors"

Session-A3

Emerging Technology and System Design (ETS-2)

Embedded Tutorial : Synthesis Techniques for Quantum Computing
Speaker **: Prof. Susmita Sur-Kolay, ISI Kolkata**

47: Bibhash Sen, Manojit Dutta, Debajyoty Banik, Dipak K Singh and Biplab K Sikdar. Design of Fault Tolerant Reversible Arithmetic Logic Unit in QCA
67: Debaprasad Das, Sourav Das and Hafizur Rahaman. Design of 4-Bit Array Multiplier using Multi-Wall Carbon Nanotube Interconnects

Session-A4

Emerging Technology and System Design (ETS-3)

Embedded Tutorial: Sample Preparation with Digital Microfluidic Biochips
Speaker: Prof. Bhargab B. Battacharya, ISI Kolkata

157: Sudip Roy, Bhargab B. Bhattacharya, Sarmishtha Ghoshal and Krishnendu Chakrabarty. Low-Cost Dilution Engine for Sample Preparation using Digital Microfluidic Biochips
104:Pranab Roy, Moudud Sohid, Sudipta Chakraborty, Hafizur Rahaman and Parthasarathi Dasgupta. System on Biochips: A new design for integration of multiple DMFBs
154: Sukanta Bhattacharjee, Ansuman Banerjee and Bhargab B. Bhattacharya. Multiple Dilution Sample Preparation Using Digital Microfluidic Biochips

Session-A5

Emerging Technology and System Design (ETS-4)
Embedded tutorial: Digital Design Using FPGA
Speaker: Prof. Susanta Sen, Calcutta University, Kolkata

33: Rohith G and Ajayan K. K. Analysis of Semiconductor Equations and Anomalous Diffusion Equation using Fractional Calculus
153:Anwesha Banerjee, Shounak Datta, Pratyusha Das, Amit Konar, D. N. Tibarewala and R. Janarthanan. Electrooculogram based Online Control Signal Generation for Wheelchair

Session-A6

Emerging Technology and System Design (ETS-5)

Embedded tutorial: Selected issues in Physical Design for Manufacturabilty
Speaker: Prof. Partha Sarathi Dasgupta, IIM Calcutta, Kolkata

59: Mamata Dalui and Biplab K Sikdar. A Test Design for Quick Determination of Incoherency in Chip Multiprocessors' Cache Realizing MOESI Protocol

52: Manodipan Sahoo and Hafizur Rahaman. Efficient and Compact Electrical Modeling of Multi Walled Carbon Nanotube Interconnects

Session-A7

Emerging Technology and System Design (ETS-6)

155: Kamalika Datta, Indranil Sengupta and Hafizur Rahaman. Particle Swarm Optimization based Circuit Synthesis of Reversible Logic

86: Prasun Ghosal and Tuhin Subhra Das. SD2D: A Novel Routing Architecture For Network-on-Chip

14: Gunda Suman, Pavan Kumar B V S, Sagar Kumar M and Chitti Babu B. Modeling, Analysis and Design of Synchronous Buck Converter using State Space Averaging Technique for PV Energy System

Session-B2

Software System and Application Design (SSD)

83: Deep Gupta, R.S. Anand and Barjeev Tyagi. Enhancement of Medical Ultrasound Images using Multiscale Discrete Shearlet Transform Based Thresholding

66:Hemant Agrawal, Sandeep Malik and Yashpal Dutta. Performance Analysis of Offloading IPsec processing to Hardware Based Accelerators

143: Jamil Galadanci, Rishad Shafik, Jimson Mathew and Amit Acharyya. A Closed-loop Control Strategy for Glucose Control in Artificial Pancreas Systems

Session-B3

Power Aware System Design (PSD)

35: Rajdeep Mukherjee, Priyankar Ghosh, Neerati Sravan Kumar, Pallab Dasgupta and Ajit Pal. Multi-Objective Low-power CDFG Scheduling using Fine-Grained DVS Architecture in Distributed Framework

19: Shashikant Sharma, Manisha Pattanaik and Balwinder Raj. Signal Stepping Based Multimode Multi-Threshold CMOS Technique for Ground Bounce Noise Reduction in Static CMOS Adders

50: Anup Anurag, Satarupa Bal and Chitti Babu B.. An improved Soft Switching DC-DC Converter for low power PV applications

Session-B5

Wireless/Wired Communication Systems (WCS)

147:Vishram Mishra, Chiew Tong Lau, Syin Chan and Ashish Kumar. Energy Aware Spectrum Decision Framework for Cognitive Radio Networks

137:Soumya Maity, Padmalochan Bera and Soumya Ghosh. Policy based ACL Configuration Synthesis in Communication Networks- a Formal Approach

136: Parthajit Roy and Jyotsna Kumar Mandal. A Delaunay Triangulation Preprocessing based Fuzzy-Encroachment Graph Clustering for Large Scale GIS Data

Poster Presentation Session

11. Utpal Nandi and Jyostna Kumar Mandal *Fractal Image Compression using Fast Context Independent HV partitioning Scheme*
25. Soumyasree Bera, Arun K Singh, Samarendra Nath Sur, Debasish Bhaskar and Rabindranath Bera, *Improvement in Target Detectability Using Spread Spectrum Radar in Dispersive Channel Condition*

26. Rekha S and Dr. Laxminidhi T, *Effect of Finite Gain and Bandwidth of feed-forward compensated OTA on Active-RC Integrators: A Case Study*
29. Kwen-Siong Chong, Idongesit Ebong,Yalcin Yilmaz, Joseph Chang and Pinaki Mazumder *Comparison of FFT/IFFT Designs Utilizing Different Low Power Techniques*
34. Ashish Gupta and Gaurav Verma, *Bridging Validation and Automatic Test Equipment (ATE) Environment*
62. Vikas Mahor, Akanksha Chauhan and Manisha Pattanaik, *A Process Variation Tolerant Low Contention Keeper Design for Wide Fan-In Dynamic OR Gate*
138. Naushad Alam, Bulusu Anand and Sudeb Dasgupta, *The Impact of Process-Induced Mechanical Stress in Narrow Width Devices and Circuit Design Issues*
140. Mousumi Saha,Souvik Das and Biplab K Sikdar, *High Speed Hardware For March C*
151. Poornima Mittal, Brijesh Kumar, Y. S. Negi and R. K.Singh*Analysis of Top and Bottom Contact Organic Transistor Performance for Different TechnologyNodes*
162. Raju Hazari, Kamalika Bhattacharjee and Sukanta Das, *Design of Hardware for Deterministic Nagel-Schreckenberg Traffic Mode*